REMARKS

This application has been carefully reviewed in light of the Office Action dated November 6, 2002. Claims 1, 11, 13, 24, 50, 62 and 73 have been amended. A marked-up version of these claims, showing changes made, is attached hereto as Appendix A. Applicants respectfully request reconsideration of the above-referenced application in light of the amendments and following remarks.

Independent claims 1, 13, 24, 50, 62 and 73 have been amended to positively recite, forming "a contact layer within said amorphous silicon layer, wherein said contact layer has a second resistance lower than said first resistance." (emphasis added). Support is found in Applicants' specification, pg. 11, lines 9-20 and FIGS. 1(d), 3(d), and 5(e).

Figures 6(a)-6(d) have been objected to under M.P.E.P. § 608.02(g). In response, a "Request for Approval of Proposed Drawing Amendments" is being filed concurrently herewith. In the request, Figures 6(a)-6(d) (described in the Discussion of the Related Art in Applicants' specification) have been labeled as "Prior Art." Accordingly, withdrawal of this objection is solicited.

Claim 11 is objected to because of an informality. In response, Claim 11 has been amended. Claim 11 now recites, that a "silicon layer is etched utilizing a common photoresist to form said electrodes." The withdrawal of this rejection is solicited.

Claims 1, 13, 24, 50, 62 and 73 stand rejected under 35 U.S.C. § 112, second paragraph as lacking sufficient antecedent basis. Claims 1, 13, 24, 50, 62 and 73 have been amended to provide a proper antecedent basis for the term "amorphous silicon layer." Withdrawal of this rejection is solicited.

Claims 1-34 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicants' Admitted Prior Art in view of Ting and Washizuka. Reconsideration is respectfully requested.

Applicants' invention relates to a novel method for forming an amorphous silicon layer having high resistance and low resistance areas. Impurity ions 5 are provided on top of the amorphous silicon layer 4 and are diffused into the amorphous silicon layer 4, forming an amorphous silicon layer 4 with two separate resistances (Figure 1(d)). Specifically, the impurity ions are diffused into the high resistance amorphous silicon layer 4 directly beneath the source and drain electrodes (Figure 1(d)) to form a low resistance contact region, e.g., a contact layer 6. The cited references do not teach this novel method.

Applicants' admitted prior art (Figures 6(a)-6(d)) teaches forming two separate layers of amorphous silicon. In particular, Applicants' prior art teaches a high resistance amorphous silicon layer 64 and a low resistance amorphous silicon layer 65. Further, Applicants' prior art does not teach providing an "impurity 65 over the amorphous silicon layer" as the Office Action asserts (Office Action, pg. 3). Layer 65, which the Office Action incorrectly designates as an impurity 65, is a second amorphous silicon layer having a low resistance (Applicants' Specification, pg. 2, lines 3-18). The "low resistance amorphous silicon layer 65 between the drain electrode 66 and the high resistance amorphous silicon layer 64 . . . is unetched and remains." The low resistance amorphous silicon layer 65 is not formed by diffusing impurities into the second amorphous silicon layer.

The Office Action further asserts that Ting teaches diffusing the impurity into the amorphous silicon layer by an annealing process. This is incorrect. Ting teaches forming a gate electrode with alternating undoped amorphous silicon layers and doped amorphous silicon layers (Col. 1, lines 50-65). Ting further teaches "a dopant such as phosphorus is in-situ doped into the second amorphous silicon layer 124." (Col. 2, lines 50-52) (emphasis added). Ting does not teach or suggest diffusing impurity ions into the amorphous silicon layer.

Moreover, Ting teaches that the phosphorus is uniformly distributed within the amorphous silicon layer. Ting's methods result in "an impurity distribution more uniform

than that of a single doped amorphous silicon layer." (Col. 3, lines 2-5) (emphasis added). This is in stark contrast to Applicants' method. Applicants teach that an area of low resistance, e.g., a contact layer 6, is formed within the amorphous silicon layer 4 as a result of diffusing impurity into the amorphous silicon layer 4. Applicants' resulting dual resistance structure could not be formed if impurities are distributed uniformly throughout the amorphous silicon layer.

The Office Action acknowledges that "Ting fails to teach the annealing temperatures and time duration as recited in present claims 6, 18, and 29." (Office Action, pg. 4). In fact, Ting teaches away from the claimed temperature range. Ting teaches that "a second amorphous silicon layer 124 doped with impurities is formed on the first amorphous silicon layer 122 [and] [t]his is carried out . . . at approximately 500° to 600° C." Dependent claims 6, 18 and 29 recite heat annealing which is "conducted at a temperature of 300°C – 320°C for about 10-15 minutes." Accordingly, Ting teaches a completely different anneal temperature from Applicants' claimed anneal temperature.

In addition, the Office Action does not comply with 35 U.S.C. § 103(a), in that it fails to explain how the thickness of the amorphous silicon layer, the concentration of impurity, and the exposure time as recited in dependent claims 2, 4, 8, 14, 16, 20, 25, 27 and 29 are rendered obvious. Indeed, the Office Action acknowledges that the Applicants' admitted prior art "fails to teach the thickness of the amorphous silicon film, the concentration of the impurity, and the exposure time as recited." (Office Action, pg. 4).

Washizuka does not rectify the deficiencies associated with Applicants' admitted prior art or Ting. Washizuka is relied upon for etching the amorphous silicon layer utilizing a common photoresist to form the electrodes. However, as provided above, Applicants' admitted prior art, even in view of Ting, does not render Applicants' invention obvious.

The cited references, even in combination, do not teach or suggest all of the limitations found in independent claims 1, 13 and 24. Specifically, the cited references fail

to teach or suggest forming "a contact layer <u>within</u> said amorphous silicon layer, wherein said contact layer has a second resistance lower than said first resistance," as recited in claims 1, 13 and 24 (emphasis added). Applicants' claimed amorphous silicon layer 4, <u>itself</u>, has two separate resistances (Figure 1(d)). Accordingly, the withdrawal of the rejection for claims 1, 13 and 24 is solicited.

Dependent claims 2-12, which includes all limitations of independent claim 1, dependent claims 14-23, which includes all of the limitations of independent claim 13, and dependent claims 25-34, which includes all of the limitations of independent claim 24, are allowable for at least those reasons set forth above with respect to independent claims 1, 13 and 24.

Claims 50-83 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicants' Admitted Prior Art in view of Ting and Washizuka.

Independent claims 50, 62 and 73 are allowable based upon the same distinctions discussed above. In particular, the cited references fail to teach or suggest forming "a contact layer <u>within</u> said amorphous silicon layer, wherein said contact layer has a second resistance lower than said first resistance," as recited in claims 50, 62 and 73 (emphasis added). Accordingly, withdrawal of the rejection of claims 50, 62 and 73 is solicited.

Dependent claims 51-61, which includes all limitations of independent claim 50, dependent claims 63-72, which includes all of the limitations of independent claim 62, and dependent claims 74-83, which includes all of the limitations of independent claim 73, are allowable for at least those reasons set forth above with respect to independent claims 50, 62 and 73.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

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APPENDIX A

1. (amended) A method of fabricating a thin film transistor comprising the steps of:

providing a gate over a substrate;

providing a gate insulating layer over said gate and said substrate;

providing [a] an amorphous silicon layer having a first resistance over said gate insulating layer;

providing an impurity over said amorphous silicon layer;

forming a drain electrode and a source electrode separated by a channel region over a contact portion with said amorphous silicon layer; and

removing said impurity from said channel region and diffusing said impurity into said contact portion to form a contact layer within said amorphous silicon layer, wherein said contact layer has a second resistance [at least] lower than said first resistance.

11. (amended) The method of claim 1 wherein said silicon layer is etched utilizing a common photoresist [used] to [formed] form said electrodes.

13. (amended) A method of fabricating a thin film transistor comprising the steps of:

providing a gate over a substrate;

providing a gate insulating layer over said gate and said substrate;

providing [a] an amorphous silicon layer having a first resistance over said gate insulating layer;

providing an impurity over said amorphous silicon layer;

etching said amorphous silicon layer utilizing a common photoresist [used] to form a drain electrode and a source electrode separated by a channel region over a contact portion with said amorphous silicon layer; and

removing said impurity from said channel region and diffusing said impurity into said contact portion to form a contact layer within said amorphous silicon layer, wherein said contact layer has a second resistance [at least] lower than said first resistance.

24. (amended) A method of fabricating a thin film transistor comprising the steps of:

providing a gate over a substrate;

providing a gate insulating layer over said gate and said substrate;

providing [a] an amorphous silicon layer having a first resistance over said gate insulating layer;

providing an impurity over said amorphous silicon layer;

providing a photoresist over said impurity [provided silicon layer] and back exposing said photoresist utilizing said gate stack as a mask and developing a pattern substantially identical with that of said gate;

removing said pattern and forming a drain electrode and a source electrode separated by a channel region over a contact portion with said amorphous silicon layer; and

removing said impurity from said channel region and diffusing said impurity

into said contact portion to form a contact layer <u>within said amorphous silicon layer,</u> wherein said contact layer has a second resistance [at least] lower than said first resistance.

50. (amended) A method of fabricating a liquid crystal display (LCD) comprising the steps of:

providing a plurality of thin film transistors arranged on a LCD substrate in a matrix form, each of said thin film transistors fabricated by the steps of:

providing a gate over a substrate;

providing a gate insulating layer over said gate and said substrate;

providing [a] <u>an amorphous</u> silicon layer having a first resistance over said gate insulating layer;

providing an impurity over said amorphous silicon layer;

forming a drain electrode and a source electrode separated by a channel region over a contact portion with said amorphous silicon <u>layer</u>; and

removing said impurity from said channel region and diffusing said impurity into said contact portion to form a contact layer <u>within said amorphous silicon layer,</u> wherein said contact layer has a second resistance [at least] lower than said first resistance.

62. (amended) A method of fabricating a liquid crystal display (LCD) comprising the steps of:

providing a plurality of thin film transistors arranged on a LCD substrate in a

matrix form, each of said thin film transistors fabricated by the steps of:

providing a gate over a substrate;

providing a gate insulating layer over said gate and said substrate;

providing [a] <u>an amorphous</u> silicon layer having a first resistance over said gate insulating layer;

providing an impurity over said amorphous silicon layer;

etching said <u>amorphous</u> silicon layer utilizing a common photoresist [used] to form a drain electrode and a source electrode separated by a channel region over a contact portion with said amorphous silicon <u>layer</u>; and

removing said impurity from said channel region and diffusing said impurity into said contact portion to form a contact layer <u>within said amorphous silicon layer,</u> wherein said contact layer has a second resistance [at least] lower than said first resistance.

73. (amended) A method of fabricating a liquid crystal display (LCD) comprising the steps of:

providing a plurality of thin film transistors arranged on a LCD substrate in a matrix form, each of said thin film transistors fabricated by the steps of:

providing a gate over a substrate;

providing a gate insulating layer over said gate and said substrate;

providing [a] <u>an amorphous</u> silicon layer having a first resistance over said gate insulating layer;

providing an impurity over said amorphous silicon layer;

providing a photoresist over said impurity [provided silicon layer] and back exposing said photoresist utilizing said gate stack as a mask and developing a pattern substantially identical with that of said gate;

removing said pattern and forming a drain electrode and a source electrode separated by a channel region over a contact portion with said amorphous silicon <u>layer</u>; and

removing said impurity from said channel region and diffusing said impurity into said contact portion to form a contact layer <u>within said amorphous silicon layer,</u> wherein said contact layer has a second resistance [at least] lower than said first resistance.